UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,901	09/11/2003	Ken Gary Pomaranski	200310430-1	5950

22879 7590 05/31/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,901	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Groups I and II in the reply filed on 3/13/06 is acknowledged. Because of the amended claim 18, applicant's argument has been found persuasive.

The requirement has been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15 31 48 and 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The phrase "substantially transparently" is unclear. Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 4, 6-9, 11-15, 18, 19, 21-26, 28-32, 34, 35, 37, 39-42, 44-49, and 52-63 are rejected under 35 U.S.C. 102(e) as being anticipated by Larson et al. U. S. Patent No. 6,832,340.

As per claim 1 Larson et al. teach the claimed system, comprising: a memory access logic configured to be operably connected to a main memory and a processor, the memory access logic comprising: a memory configured to store contents of a main memory location and to accept memory access requests for the main memory location from the processor while the contents of the main memory location are stored in the memory; and a scrub logic configured to selectively mirror the main memory location into the memory and to selectively scrub the main memory location. (column 7 lines 25-30)

As per claims 2, Larson et al. teach the memory access logic comprises an ASIC. (Column 3 line 14)

As per claim 4, Larson et al. teach a second memory configured to store one or more configuration parameters associated with scrubbing the main memory location, and where the scrub logic is further configured to selectively scrub the main memory location based, at least in part, on one or more of the configuration parameters. (Column 4 line 3-5)

As per claim 6, Larson et al. teach the second memory is writeable by an application located external to the memory access logic. (Column 3 lines 40-42)

As per claim 7, Larson et al. teach the second memory stores one or more of, an on/off parameter, an address of a main memory location to be scrubbed, a starting address of a range of main memory locations to be scrubbed, an ending address of the range of main memory locations to be scrubbed, a rate parameter associated with the rate at which main memory scrubbing is to occur, and a log configuration parameter. (Column 7 lines 16-22)

As per claim 8, Larson et al. teach the log configuration parameter stores one or more entry point addresses for one or more logging processes. (Column 7 lines 40-45)

As per claim 9, Larson et al. teach a log configured to store a result value associated with scrubbing the main memory location, and where the scrub logic is further configured to selectively produce the result value. (Column 3 lines 54-55, and column 7 lines 20-23)

As per claims 11, 14, 39, and 46, Larson et al. teach the log is readable (writeable) by an application located external to the memory access logic. (Column 3 lines 19-22)

As per claim 12, Larson et al. teach the scrub logic is configured to selectively generate a signal when the main memory location that is being scrubbed exhibits a memory error. (Column 6 lines 23-25)

As per claim 13, and 45, Larson et al. teach the scrub logic is configured to initiate scrubbing the main memory location by sending one or more signals to an

onboard memory testing logic, where the onboard memory testing logic is physically connected to the main memory location. (Column 5 lines 41-45)

As per claim 15, 48 and 49, Larson et al. teach the scrub logic is configured to scrub the main memory location substantially transparently to operating system control (inherent) of main memory. (Column 3 lines 10-15)

As per claim 18, Larson et al. teach a fault management logic configured to selectively process a memory fault associated with the main memory location. (Column 6 lines 18-22)

As per claim 19, Larson et al. teach the memory access logic comprises an ASIC. (Column 3 lines 14-16)

As per claim 21, Larson et al. teach a second memory configured to store one or more configuration parameters associated with the fault management processing of the main memory location, and where the fault management logic is further configured to selectively process the memory fault based, at least in part, on the configuration parameters. (Column 3 line 30-35)

As per claim 22, Larson et al. teach the second memory comprises one or more registers. (Column 4 lines 8-10)

As per claim 23, Larson et al. teach the second memory is writeable by an application located external to the memory access logic. (Column 3 line 36-38)

As per claim 24, Larson et al. teach the second memory stores one or more of, an on/off parameter, an address of a main memory location for which fault management processing is to be performed, a starting address of a range of main memory locations for which fault management processing is to be performed, an ending address of the range of main memory locations for which fault management processing is to be performed, a rate parameter associated with the rate at which main memory fault management processing is to occur, and a log configuration parameter. (Column 3 lines 42-44)

As per claims 25, and 41, Larson et al. teach the log configuration parameter stores one or more entry point addresses for one or more fault management processes. (Column 7 lines 40-43)

As per claim 26, Larson et al. teach a log configured to store a result value associated with fault management processing of a memory fault experienced by the main memory location, and where the fault management logic is further configured to selectively produce the result value. (Column 7 lines 43-47)

As per claims 28, and 44, Larson et al. teach the log is readable by an application external to the memory access logic. (Column 7 lines 43-47)

As per claim 29, Larson et al. teach the fault management logic is configured to selectively generate a signal when the main memory location exhibits a memory fault. (Column 7 lines 43-47)

As per claims 30, and 47, Larson et al. teach the fault management logic is writeable by an application external to the memory access logic. (Column 7 lines 40-51)

As per claim 31, Larson et al. teach the fault management logic is configured to perform fault management processing for the main memory location substantially transparently to operating system control of main memory. (Column 3 lines 10-15)

As per claims 32, and 52, Larson et al. teach the fault management logic is further configured to perform one or more of, selectively logging data associated with the memory fault, selectively attempting to correct the memory fault, selectively logically removing the main memory location from the main memory, and selectively halting the operation of a computer with which the system is associated. (Column 7 lines 40-51)

As per claims 34, and 53, Larson et al. teach a main memory controller configured to be operably connected to a main memory and a processor, the main memory controller comprising: a memory configured to logically replace one or more main memory locations; a scrub logic configured to selectively scrub the one or more main memory locations; and a fault management logic configured to selectively process a memory fault generated by the one or more main memory locations. (Column 6 lines 40-50)

As per claim 35, Larson et al. teach the main memory controller comprises an ASIC. (Column 3 lines 14-16)

As per claim 37, Larson et al. teach a second memory configured to store one or more configuration parameters associated with scrubbing the one or more main

memory locations or processing a memory fault generated by the one or more main memory locations, where the scrub logic is further configured to selectively scrub the main memory locations based, at least in part, on one or more of the configuration parameters, and where the fault management logic is further configured to selectively process a memory fault generated by the main memory locations based, at least in part, on one or more of the configuration parameters. (Column 4 lines 3-5)

As per claim 40, Larson et al. teach the second memory stores one or more of, one or more on/off parameters, an address of a main memory location to be scrubbed, a starting address of a range of main memory locations to be scrubbed, an ending address of the range of main memory locations to be scrubbed, a rate parameter associated with the rate at which main memory scrubbing is to occur, an address of a main memory location for which fault management processing is to be performed, a start address of a range of main memory locations for which fault management processing is to be performed, an ending address of the range of main memory locations for which fault management processing is to be performed, and a log configuration parameter. (Column 7 lines 16-22)

As per claim 42, Larson et al. teach a log configured to store a result value associated with scrubbing the main memory locations or processing a memory fault generated by the main memory locations and where the fault management logic is further configured to selectively produce the result value. (Column 7 lines 43-47)

As per claim 54, Larson et al. teach the fault management processing includes one or more of, selectively logging data associated with the memory fault, selectively attempting to correct the memory fault, selectively logically removing the main memory location from the main memory, and selectively halting the operation of a system to which the main memory controller chipset is operably connected. (Column 7 lines 31-51)

As per claim 55, Larson et al. teach the main memory location can be scrubbed or tested by one or more of, writing back corrected data to the memory location, a parity test, an electrical test, a striping test, a marching ones test, a marching zeroes test, and a pattern test. (Column 4 lines 28-41)

As per claims 56, 57, 60, and 63, Larson et al. teach a system and technique for correcting data errors in a memory device. More specifically, data errors in a memory device are corrected by scrubbing the corrupted memory device. Generally, a host controller delivers a READ command to a memory controller. The memory controller receives the request and retrieves the data from a memory sub-system. The data is delivered to the host controller. If an error is detected, a scrub command is induced through the memory controller to rewrite the corrected data through the memory sub-system. Once a scrub command is induced, an arbiter schedules the scrub in the queue. Because a significant amount of time can occur before initial read in the scrub write back to the memory, an additional controller may be used to compare all subsequent READ and WRITE commands to those scrubs scheduled in the queue. If a memory location is rewritten with new data prior to scheduled scrub corresponding to

the same address location, the controller will cancel the scrub to that particular memory location. (Abstract, column 11 ine48 through column 12 lines7, column 12 line 53 through column 23 line14)

As per claims 58, 59, 61, and 62, Larson et al. teach the memory management operations include memory scrubbing and fault processing. (Abstract)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 3, 5, 10, 16, 17, 20, 27, 33, 36, 38, 43, 50, and 51are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson et al. U. S. Patent No. 6,832,340.

As per claims 3, 20, and 36, Larson et al. teach the memory access logic comprises a PROM. (Column 3 line 65) The examiner would like to point out that a DRAM is a functional equivalent to PROM and is therefore an obvious design choice as both were well known in the art at the time this invention was made.

As per claims 5, 10, 27, 38, and 43, Larson et al. teach cache instead of registers however cache is also the functional equivalent of a register and is therefore an obvious design choice as both were well known in the art at the time this invention was made. (Column 4 lines 8-12) (Column 7 lines 40-43)

As per claims 16, and 50, Larson et al. teach the system is embedded in a computer. (Figure 3 elements 30-35) as per the use of memory control device would imply that a computer is using the device and is therefore an obvious design choice as both were well known in the art at the time this invention was made.

As per claims 17, 33, and 51, Larson et al. teach the system is embedded in an image-forming device. (Figure 3 elements 30-35) the ultimate placement of a device is

therefore an obvious design choice as both were well known in the art at the time this invention was made.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt
Examiner
Art Unit 2138